**ABSTRACT OF THE DISCLOSURE**

Disclosed is a technique capable of enhancing the degree of freedom in the layout of a rerouting layer in a wafer level CSP in which defect repairing is performed by cutting a fuse. More specifically, after the defect repairing is performed by irradiating a laser beam to a fuse, an organic passivation layer (photo-sensitive polyimide layer) is filled in a fuse opening. Thereafter, a rerouting layer, a bump land, an uppermost wiring layer, and a solder bump are formed on the organic passivation layer. In the following steps of the defect repairing, the baking process to cure an elastomer layer and the uppermost protection layer is conducted at a temperature below 260°C in order to prevent the variance of the refresh times of memory cells.